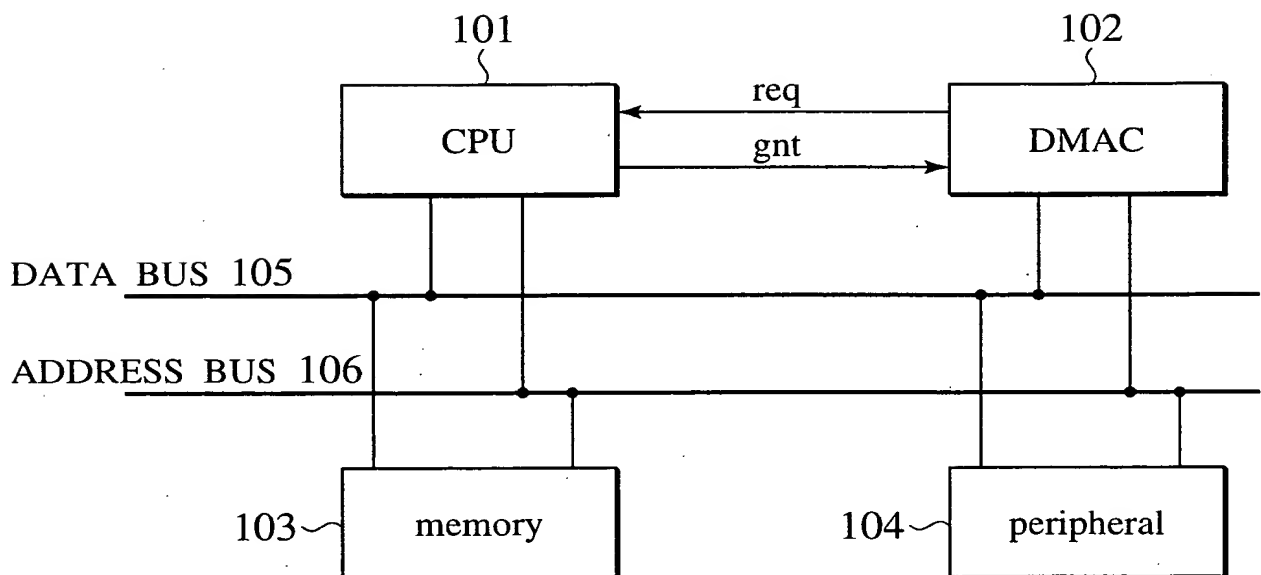
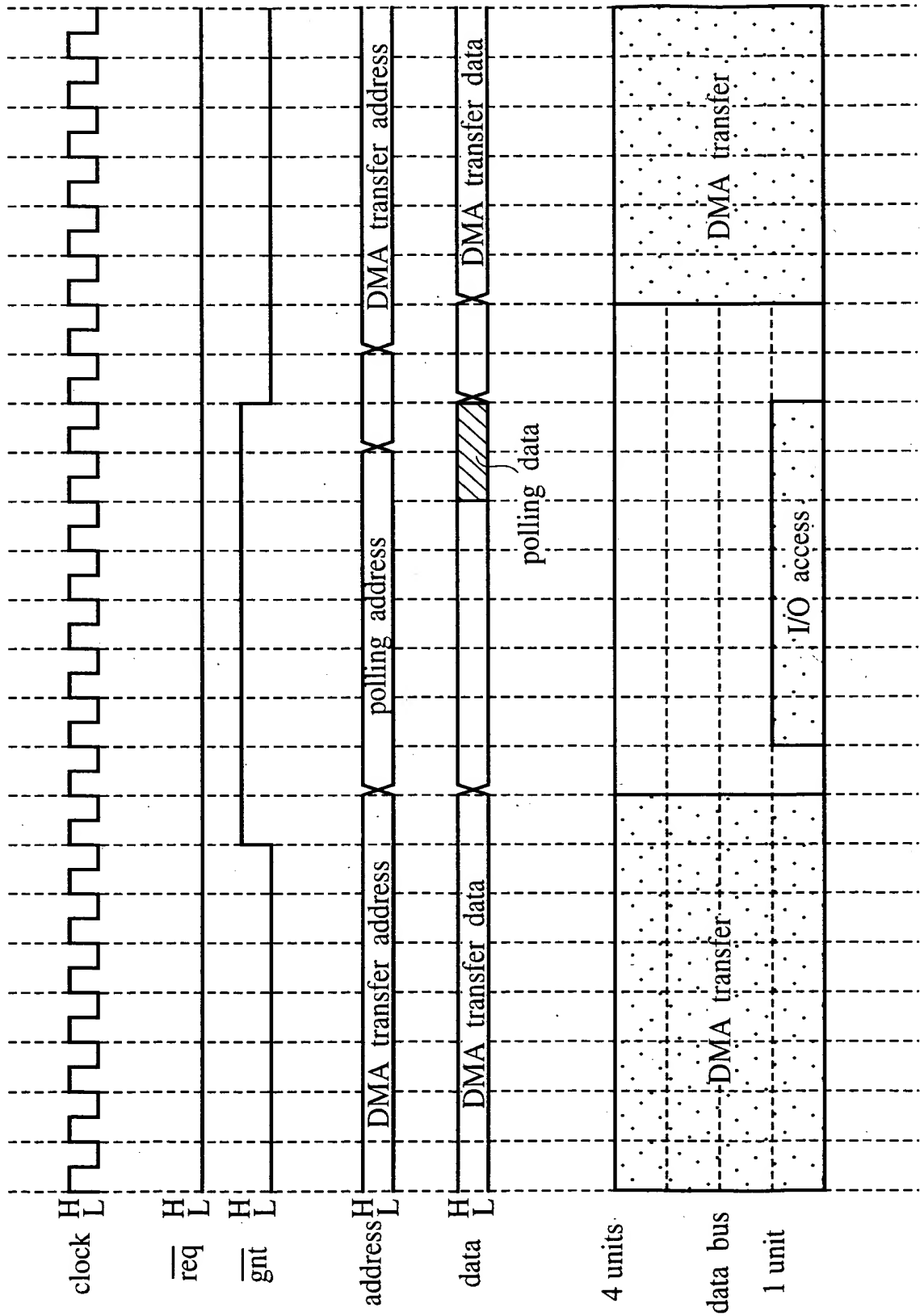


FIG.1
PRIOR ART



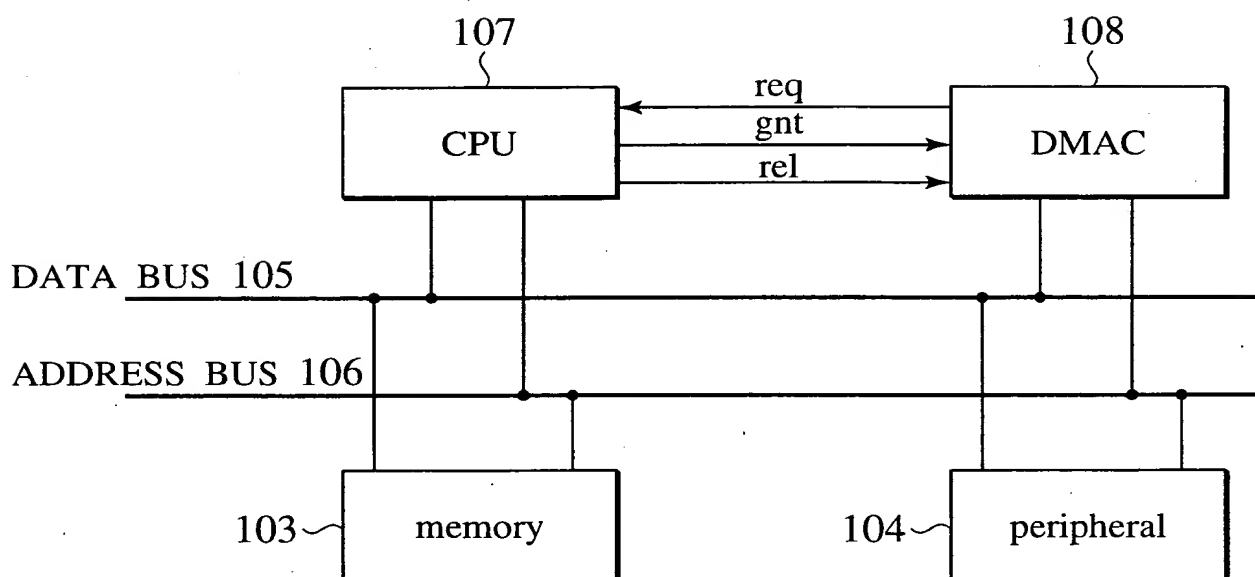
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FIG. 2
PRIOR ART



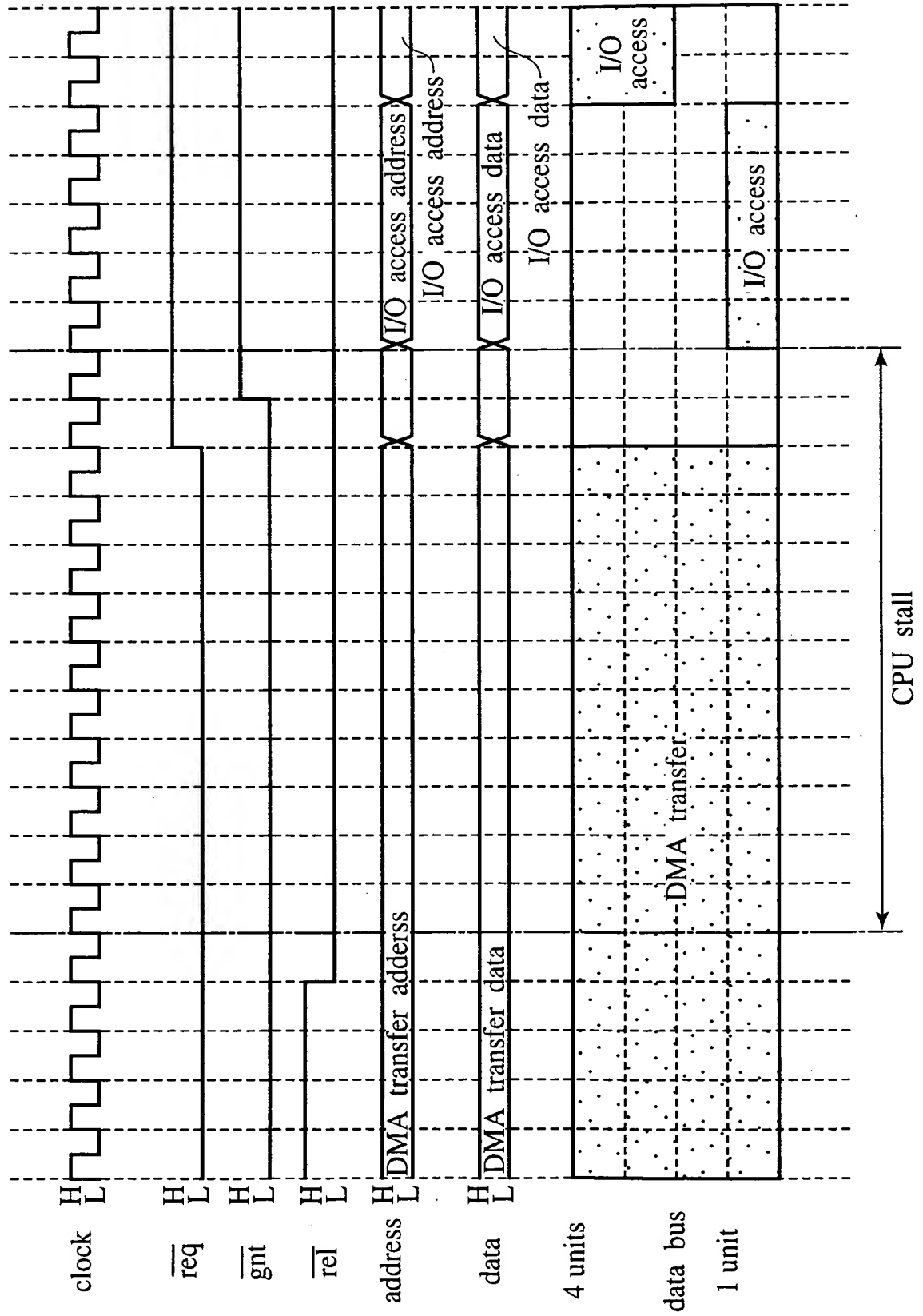
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FIG.3
PRIOR ART

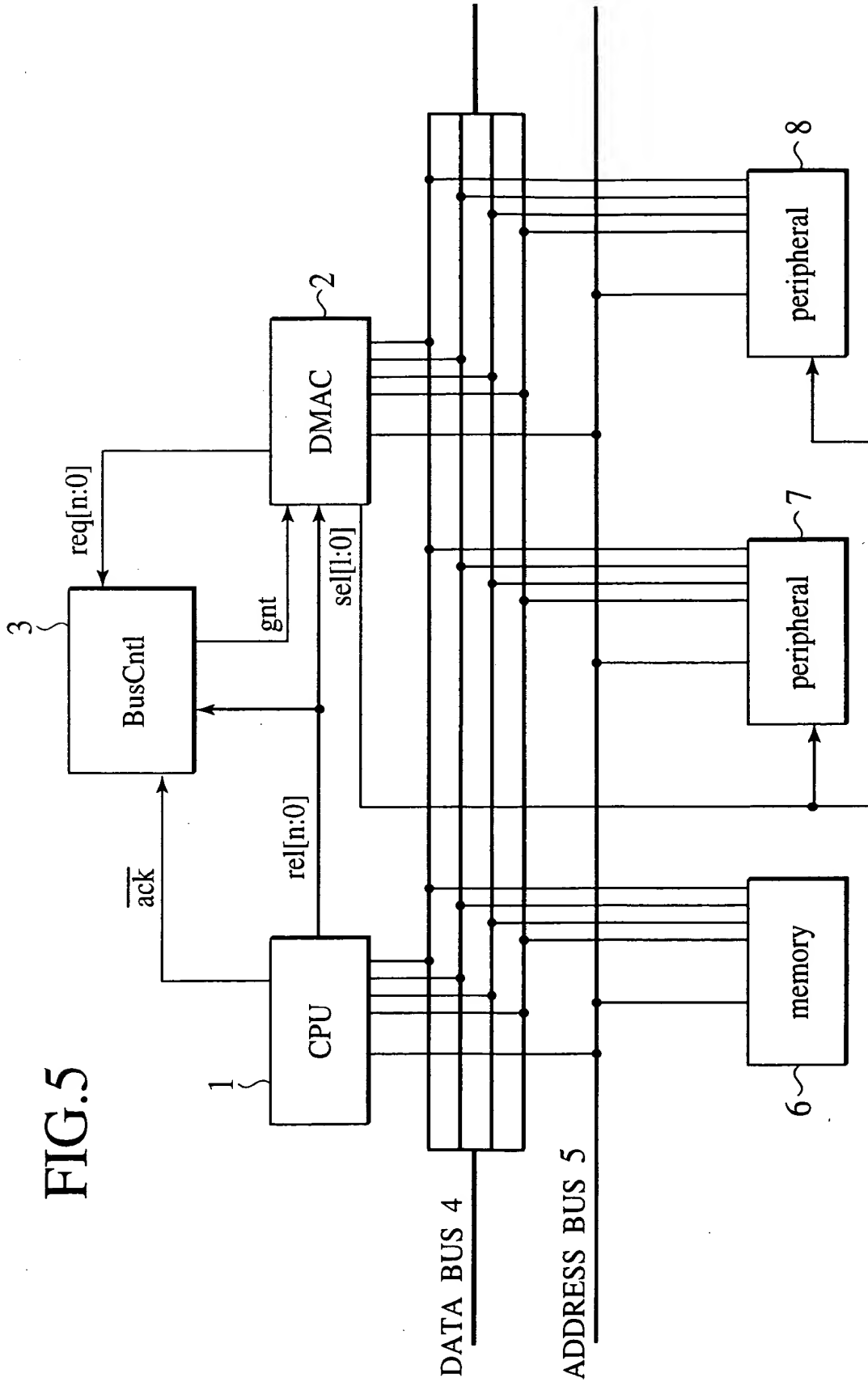


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FIG.4
PRIOR ART

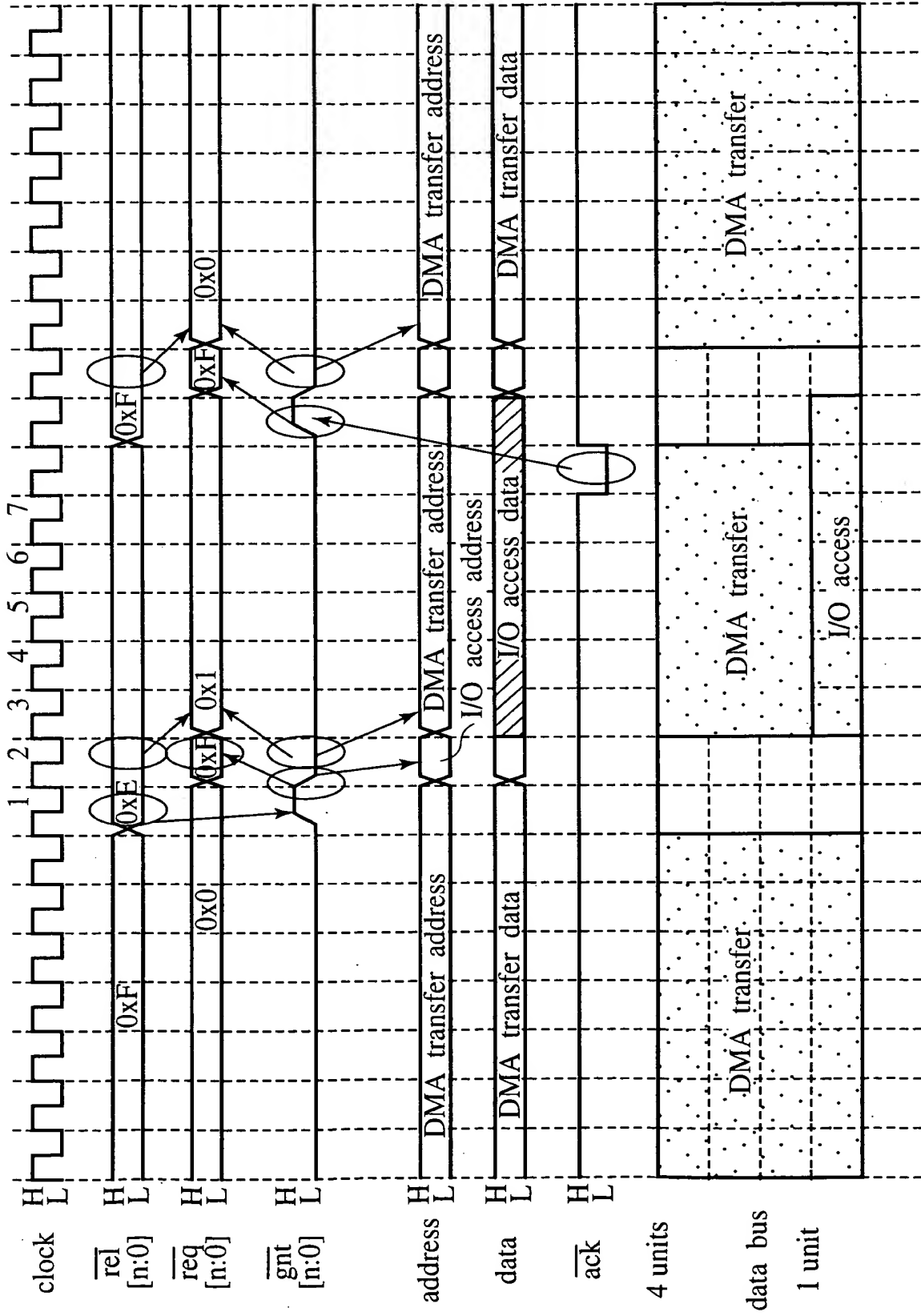


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FIG.6



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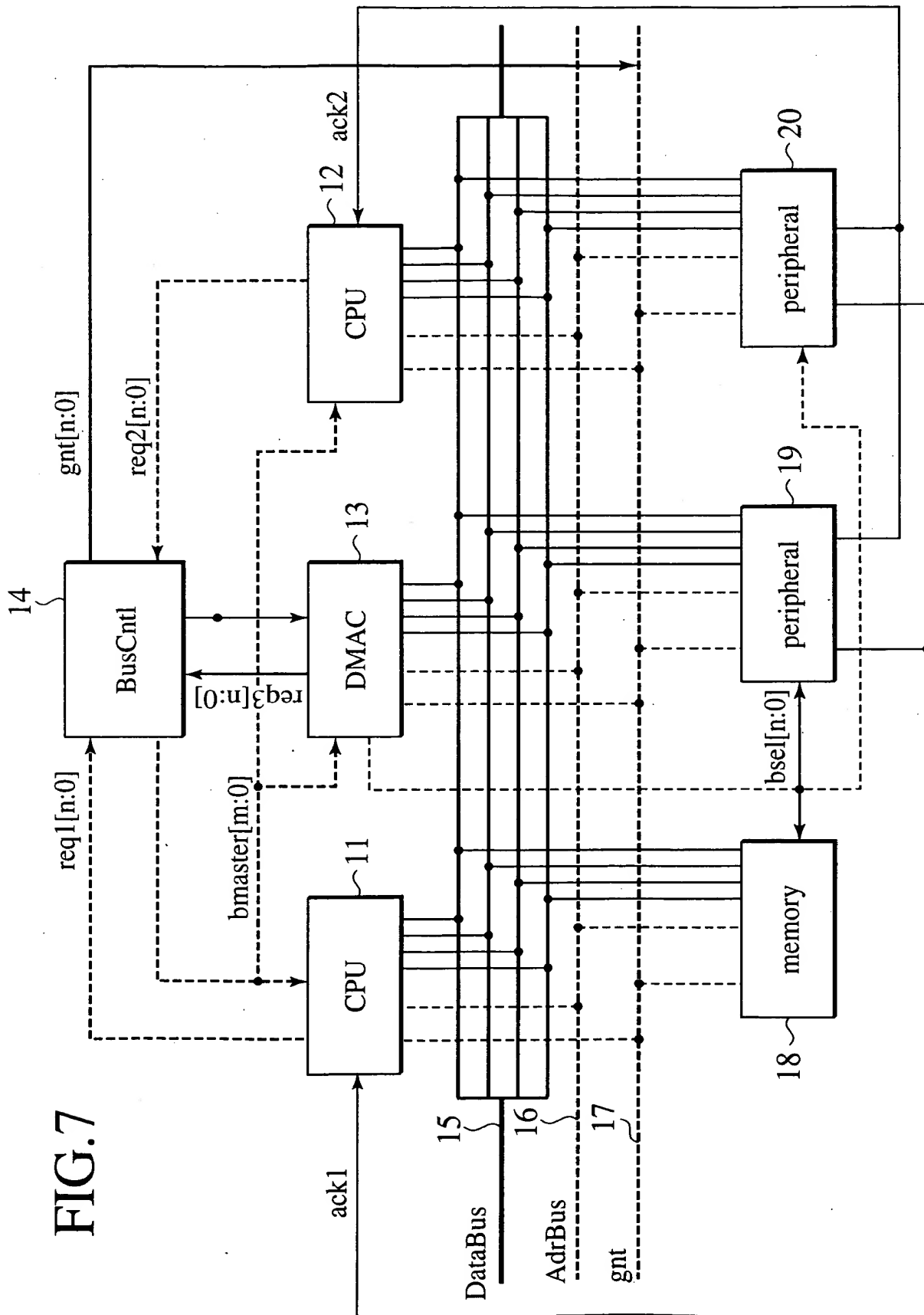
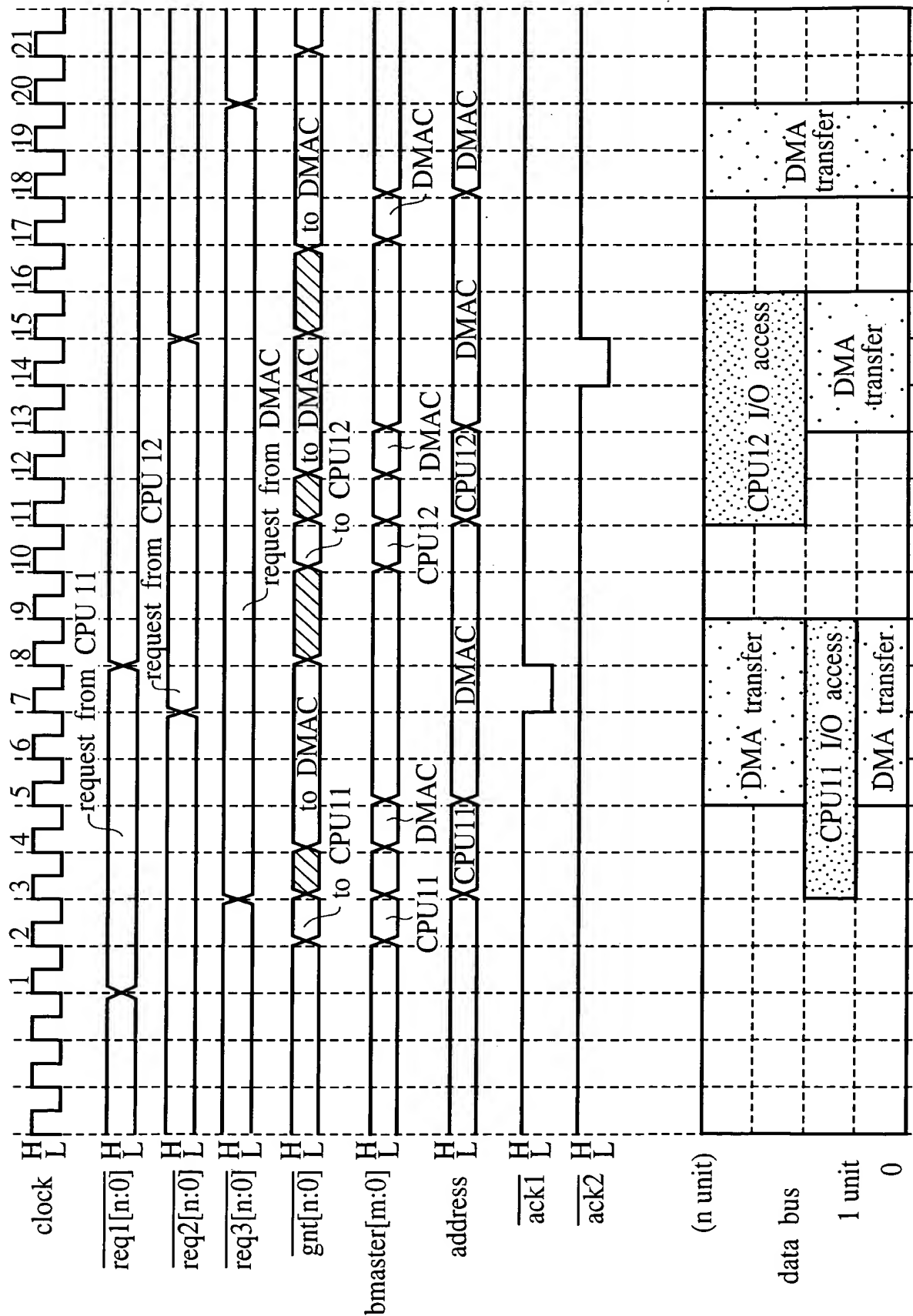


FIG. 7

FIG. 8



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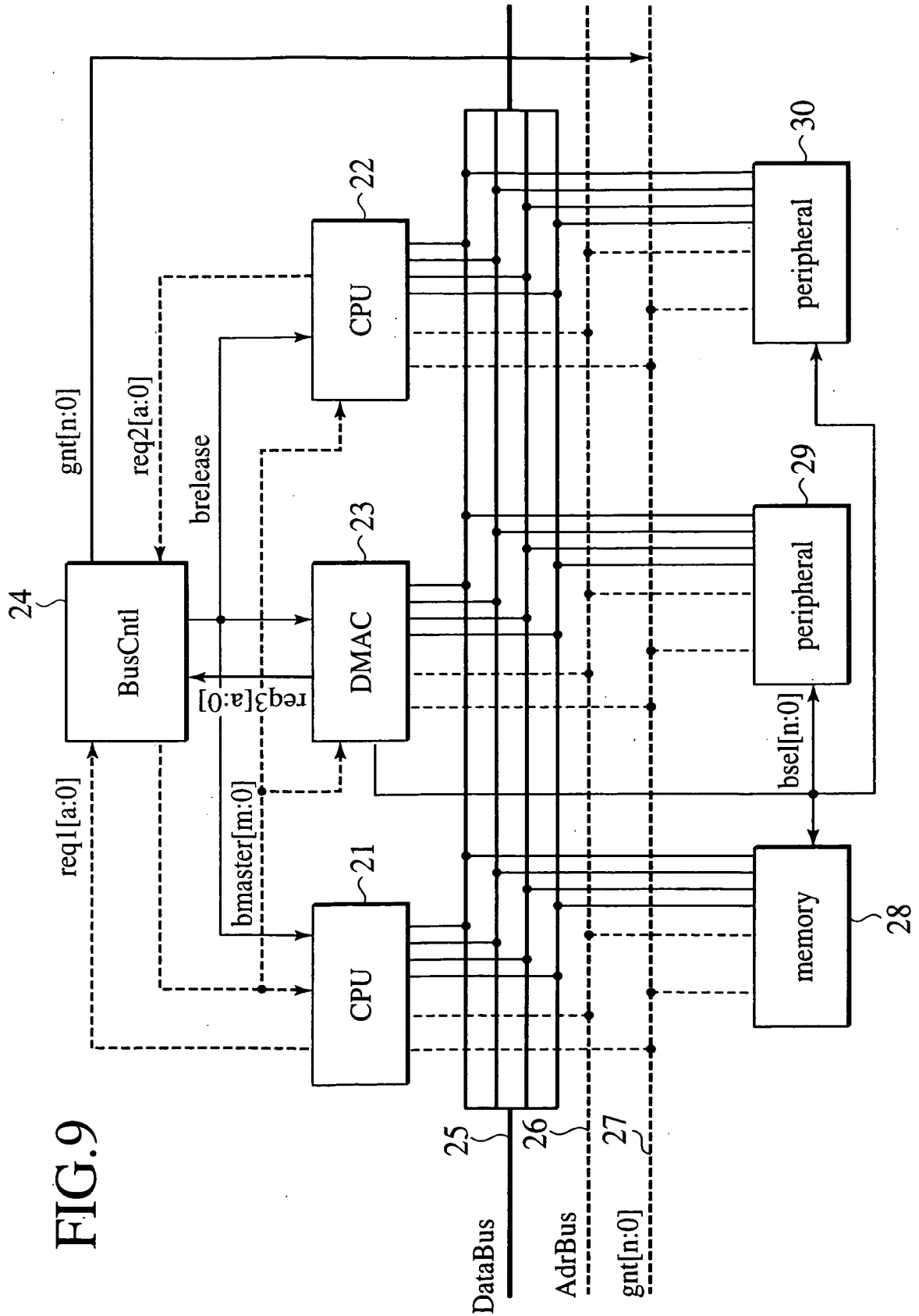
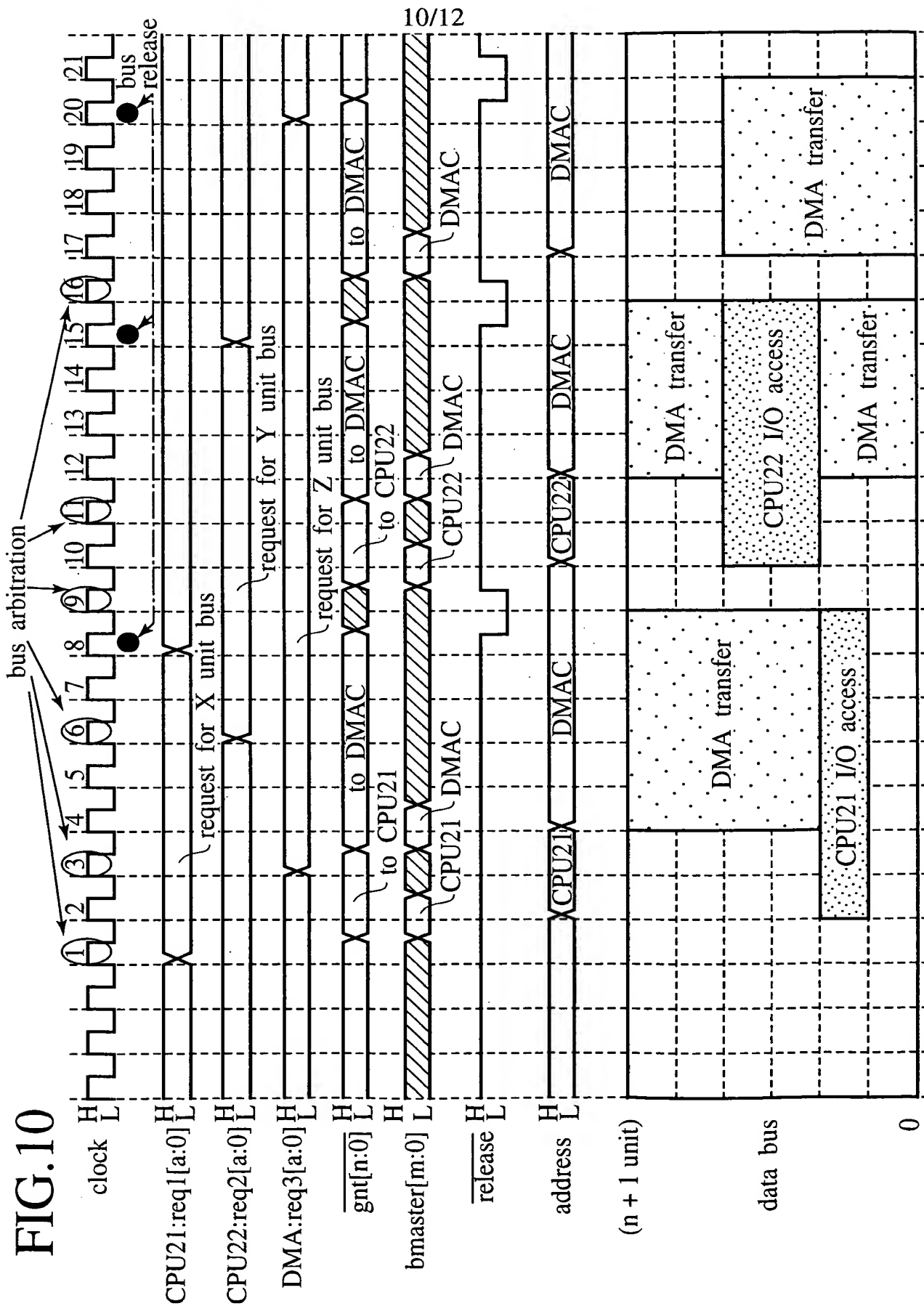


FIG.10



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FIG. 11

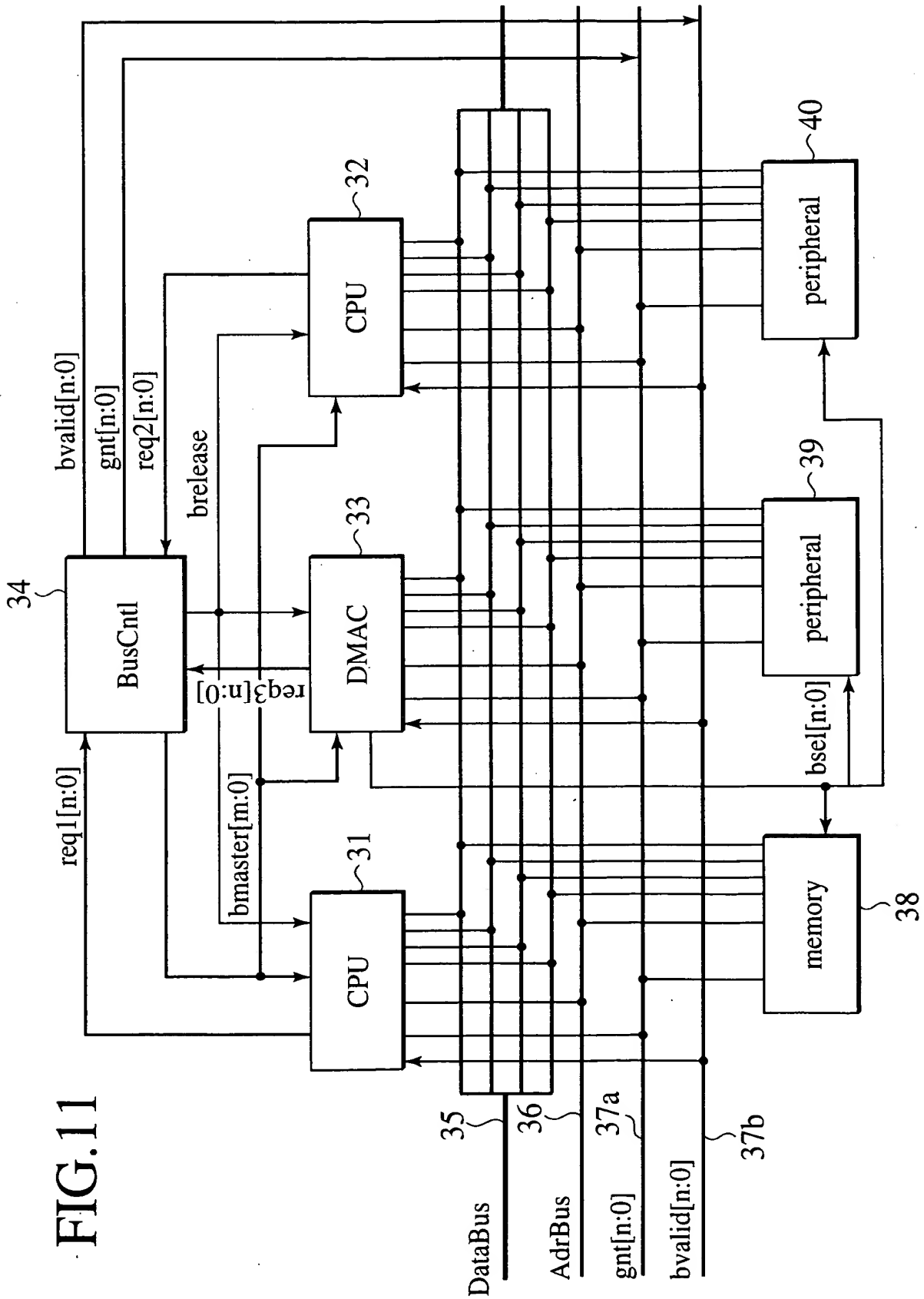


FIG. 12

The diagram illustrates a bus arbitration sequence over 21 clock cycles. The clock signal is shown at the top, with cycles numbered 1 through 21. The bus is initially in a high state. At cycle 1, CPU31 requests the bus. At cycle 2, CPU32 requests the bus. At cycle 3, CPU31 requests the bus again. At cycle 4, CPU32 requests the bus again. At cycle 5, CPU31 requests the bus again. At cycle 6, CPU32 requests the bus again. At cycle 7, CPU31 requests the bus again. At cycle 8, CPU32 requests the bus again. At cycle 9, CPU31 requests the bus again. At cycle 10, CPU32 requests the bus again. At cycle 11, CPU31 requests the bus again. At cycle 12, CPU32 requests the bus again. At cycle 13, CPU31 requests the bus again. At cycle 14, CPU32 requests the bus again. At cycle 15, CPU31 requests the bus again. At cycle 16, CPU32 requests the bus again. At cycle 17, CPU31 requests the bus again. At cycle 18, CPU32 requests the bus again. At cycle 19, CPU31 requests the bus again. At cycle 20, CPU32 requests the bus again. At cycle 21, CPU31 requests the bus again. The bus is released at cycle 21.

The diagram shows the following signals and their states over time:

- clock**: A periodic square wave signal.
- CPU31:req1[n:0]**: Request signal for CPU31, active (H) during cycles 1, 3, 5, 7, 9, 11, 13, 15, 17, 19, and 21.
- CPU32:req2[n:0]**: Request signal for CPU32, active (H) during cycles 2, 4, 6, 8, 10, 12, 14, 16, 18, and 20.
- DMA:req3[n:0]**: Request signal for DMA, active (H) during cycles 1, 3, 5, 7, 9, 11, 13, 15, 17, 19, and 21.
- gnt[n:0]**: Grant signal, active (H) during cycles 1, 3, 5, 7, 9, 11, 13, 15, 17, 19, and 21.
- bmaste[m:0]**: Master signal, active (H) during cycles 1, 3, 5, 7, 9, 11, 13, 15, 17, 19, and 21.
- address**: Address signal, active (H) during cycles 1, 3, 5, 7, 9, 11, 13, 15, 17, 19, and 21.
- release**: Release signal, active (H) during cycles 1, 3, 5, 7, 9, 11, 13, 15, 17, 19, and 21.
- bvalid[n:0]**: Valid signal, active (H) during cycles 1, 3, 5, 7, 9, 11, 13, 15, 17, 19, and 21.

The data bus activity is shown in the bottom section of the diagram:

- (n + 1 unit)**: DMA transfer during cycles 1-4, 5-8, 9-12, 13-16, 17-20, and 21.
- data bus**: CPU31 I/O access during cycles 1-4, 5-8, 9-12, 13-16, 17-20, and 21.
- 0**: CPU32 I/O access during cycles 1-4, 5-8, 9-12, 13-16, 17-20, and 21.

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